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09/712,104	11/14/2000	Masaki Sano	NEC 177	9234
27667	7590	08/21/2006	EXAMINER	
HAYES, SOLOWAY P.C. 3450 E. SUNRISE DRIVE, SUITE 140 TUCSON, AZ 85718			CHU, KIM KWOK	
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			2627	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1 and 2 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Nogawa (U.S. Patent 6,147,530) in view of Vitiello et al. (U.S. Patent 4,918,404).

Nogawa teaches a PLL circuit very similar to that of the present invention as cited in Claim 1. For example, Nogawa teaches the following:

(a) With respect to Claim 1, a phase comparator 1 detecting a phase difference (Fig. 8); a charge pump 7, 8, 10 converting the phase difference into a voltage (Fig. 8); a loop filter 3, 4, smoothing the voltage (Fig. 8); a voltage-controlled oscillator 5 receiving the smoothed voltage as a control voltage (Fig. 8); the phase comparator 1 compares phase of an output signal from the voltage-controlled oscillator 5, or phase of an output signal obtained by frequency-dividing the output of the voltage-controlled oscillator by a frequency

divider 6 to an input signal (Fig. 8); wherein the voltage-controlled oscillator 5 has a non-inverting input terminal and an inverting input terminal (Fig. 8; inherent feature); the non-inverting input terminal (+) has a variable terminal voltage VC (Fig. 8); the voltage-controlled oscillator 5 has a difference voltage VC between terminal voltages impressed upon respective ones of the non-inverting and inverting input terminals is input to the voltage-controlled oscillator as a control voltage so that the voltage-controlled oscillator 5 oscillate at a frequency in accordance with this control voltage (Fig. 8; different voltage VC is applied between terminals of the VCO 5); the charge pump 7, 8, 10 controls enlarging or reducing the difference voltage between both variable terminal voltages VC of non-inverting and inverting input terminals of the voltage-controlled oscillator 5 in accordance with an output from the phase comparator 1 representing the result of the phase comparison (Fig. 8; variable voltage VC is applied to both the variable terminals of the VCO 5).

However, Nogawa does not teach that the inverting input terminal (-) has a variable terminal voltage.

Vitiello teaches that the inverting input terminal (-) has a variable terminal voltage VRANGE (Figs. 2-4).

The frequency response characteristics of a voltage-controlled oscillator (VCO) varies from unit to unit especially under temperature variations. In this case, a fixed reference voltage V_{ref} applied to inverting input of Nogawa's VCO cannot assure correct and reliable operation. Hence, it would have been obvious to one of ordinary skill in the art to apply Vitiello's variable $VRANGE$ to the inverting terminal of Nogawa's VCO, because the input $VRANGE$ periodically adjusted the VCO so that the VCO is independent of thermal drift.

(b) With respect to Claim 2, Nogawa further teaches that the charge pump 7, 8, 10 controls (i) enlarging the difference voltage by raising the terminal voltage of the non-inverting input terminal and lowering the terminal voltage of the inverting input terminal of the voltage controlled oscillator 5 in accordance with the output from the phase comparator 1 (Fig. 8; one terminal always has higher voltage than the other terminal); or (ii) reducing the difference voltage by lowering the terminal voltage of the non-inverting input terminal and raising the terminal voltage of the inverting input terminal of the voltage-controlled oscillator in accordance with the output from the phase comparator 1 (Fig. 8; one terminal always has higher voltage than the other terminal).

Allowable Subject Matter

3. Claims 23-43 are allowable over prior art.

4. Claim 3 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. The following is an Examiner's statement of reasons for the indication of allowable subject matter:

As in claims 3 and 23, the prior art of record fails to teach or fairly suggest a PLL circuit having the following features:

(a) first and second loop filters connected at output terminals to the non-inverting and inverting input terminals, respectively, of the voltage-controlled oscillator;

(b) the charge pump performs the following control that in accordance with an output from the phase comparator representing the result of the phase comparison, a first capacitor a terminal voltage whereof provides an output terminal voltage of the first loop filter is charged to thereby raise the terminal voltage of the non-inverting input terminal of the voltage-controlled oscillator, and a second capacitor a terminal voltage whereof provides an output terminal voltage of

terminal voltage of the inverting input terminal of the voltage-controlled oscillator, whereby the difference voltage is enlarged at the time of an operation for raising the oscillation frequency of the voltage-controlled oscillator; and

(c) the charge pump performs the following control that in accordance with the output from the phase comparator representing the result of the phase comparison, the first capacitor is discharged to thereby lower the terminal voltage of the non-inverting input terminal of the voltage-controlled oscillator, and the second capacitor is charged to thereby raise the terminal voltage of the inverting input terminal of the voltage-controlled oscillator, whereby the difference voltage is reduced at the time of an operation to lower the oscillation frequency of the voltage-controlled oscillator.

The features indicated above, in combination with the other elements of the claims, are not anticipated by, nor made obvious over, the prior art of record.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Ogasawara (5,574,515) is pertinent because Ogasawara teaches a VCO circuit.

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.


8. Any inquiry concerning this communication or earlier communication from the examiner should be directed to Kim CHU whose telephone number is (571) 272-7585 between 9:30 am to 6:00 pm, Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William Korzuch, can be reached on (57) 272-7589.

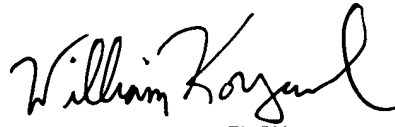
The fax number for the organization where this application or proceeding is assigned is (571) 273-8300

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Kim-Kwok CHU

 8/16/06
Examiner AU2627
August 16, 2006

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